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Super Capacitor Based Multilevel Inverter for Traction Control System

P. Srinivasan[1,*], K. Arulvendhan[2], Amal Babu[3]

[1]Department of Electrical and Electronics, Saveetha Engineering College, Thandalam, Chennai, Tamil Nadu, India.
[2,3]Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Ramapuram, Chennai, Tamil Nadu, India.
srinivasp808@gmail.com[1], arulvenk@srmist.edu.in[2], amal.babu35@gmail.com[3]

*Corresponding author

Abstract: This study examines the integration of a supercapacitor-based multilevel inverter within a traction control system, with a focus on its operational control strategies. A combined model incorporating traction control dynamics and forecasting of power generation from the supercapacitor is developed to optimize inverter operation and support real-time energy scheduling. The study introduces a droop control method specifically designed for power electronic converters interfaced with battery storage, thereby enhancing voltage regulation and load sharing in dynamic environments. Simulation models are created using LT Spice/ Simulink to evaluate three configurations: an open-loop super capacitor system, a closed-loop system using PID control, and a hybrid system combining super capacitors with a PID-controlled multilevel inverter. Comparative analysis of these models reveals that the PID-based inverter system significantly outperforms the others in terms of response speed, voltage regulation, and system stability. The closed-loop control enables more accurate handling of transient conditions, reducing voltage sag and improving current regulation. Furthermore, the system demonstrates reduced hardware complexity, offering a compact and cost-effective solution suitable for traction applications. By leveraging the rapid charge-discharge characteristics of super capacitors along with the fine-tuned control capabilities of PID algorithms, the proposed system ensures reliable and efficient traction performance under variable load conditions.

Keywords: Super Capacitor; Multilevel Inverter; PI and PID Controller; LT Spice/Simulink; Response Speed; Hardware Complexity; Cost-Effective; Traction Control Technology; Pulse Width Modulation.

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1. Introduction

Advancements in traction control technology and the growth of notebook computer machines and other battery-powered equipment have driven the increasing demand for compact, dependable multilevel inverters. These switching inverters, more often referred to as multilevel inverters, employ a matrix of semiconductor switches to monitor and convert raw input power into a regulated output with minimal delay. The core of this regulation is the switching strategy, which is under significant control through Pulse Width Modulation (PWM). PWM is a common technique in which a constant switching frequency and a variable duty cycle control the switching operation. The duty cycle, being the ON-time of the switch divided by the switching period ratio, provides accurate control of the output characteristics of the inverter. Multilevel inverters can operate in two

modes: Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM). In CCM, the inductor current never falls to zero during a full switching cycle; therefore, there is uninterrupted energy transfer. The uninterrupted flow of current makes CCM suitable for high-efficiency and low-ripple applications. Conversely, DCM allows the inductor current to decline to zero at the end of the switch period, which typically leads to increased losses and a larger output voltage ripple (OVR). The OVR is a crucial parameter that impacts the quality of the inverter output, as well as the operation of the load, particularly in cases involving delicate electronic and motor control loads.

OVR predominantly results from repeated charging and discharging of the output capacitor through the ON-OFF transitions of the switch and the counter transition of the switch, respectively. The frequency and amplitude of this ripple depend on several factors, like the value of the output capacitor, the inductor characteristics, the switching frequency of the converter, and the dynamic properties of the control circuit. Among these, one important one is the output capacitor's Equivalent Series Resistance (ESR). High ESR helps increase the magnitude of ripple, whereas capacitors with low ESR reduce it. Hence, for the inverter to run at its best, capacitors with minimum ESR should be used. To further minimise OVR, as well as to improve the inverter output quality, an LC filter consisting of an inductor and a capacitor is commonly placed in the output stage. The inductor primarily functions to remove current ripple, while the capacitor serves to remove voltage ripple.

The LC filter design must consider the required output voltage, current waveform, switching frequency, and allowable ripple. However, the traditional capacitors used in LC filters are bulky, which contributes to the increased size and weight of the inverter system. For the solution of the above problems, supercapacitors have been proposed as a viable candidate. Supercapacitors have greater energy density and better dynamic response than conventional electrolytic capacitors. Supercapacitors are capable of withstanding fast charge-discharge cycles and are thus well-suited for use in high-frequency inverters. Additionally, their low inherent ESR offers the potential for very low OVR. Miniature supercapacitor utilization has been especially beneficial in interleaved converter topologies, where several inverters are distributed across a common core. Interleaving not only loads thermal and electrical stress more uniformly but also decreases the overall system weight, size, and cost of the inverter. It also minimises inductor and capacitor ripple currents, resulting in improved transient response.

Along with hardware optimisation, various advanced voltage control schemes have also been implemented to minimise the output voltage ripple in multilevel inverter modules. Voltage-lifting is one of them, which enhances the level of the output voltage without increasing the input supply. This is particularly beneficial in positive output supercapacitor-based inverter topologies, as the circuit achieves high efficiency, high power density, and low ripple behavior. Voltage-lifting methods employed in diode-clamped and flying capacitor multilevel inverters have also yielded satisfactory results, enabling effective voltage conversion with low ripple. Another dominant ripple mitigation technique is the Sliding Mode Current Control (SMCC) technique. SMCC is a nonlinear control technique with parameter robustness and disturbance insensitivity. SMCC regulates the system to 'slide' along a designed path, thus ensuring stable operation and minimum output ripple even under dynamic load conditions. Another promising technique in quasi-PWM multilevel inverters is Automatic Loop-Bandwidth (ALB) control. With varying loop bandwidth, ALB can provide a high transient response and accurate PWM control, thereby minimizing output ripple.

Incorporating hysteresis control further enhances this function, allowing for quick adjustment of the deviation from the desired output. The typical disadvantage in multilevel inverters that work in the CCM is that the transfer function contains a right-half plane zero (RHPZ). The RHPZ causes phase lag, makes it difficult to design the compensation circuit for feedback loops, and reduces the maximum controllable bandwidth of the control system. Although it helps to provide an excellent theoretical transient response, the actual implementation becomes complex because of stability issues. To counter this, a newly developed non-isolated multilevel inverter topology, known as the Cascaded H-Bridge (CHB) inverter, has emerged. The CHB inverter has the merits of diode-clamped and synchronous rectified flying capacitor inverters. The CHB inverter is usually made up of two capacitors – one on the input and one on the output connected to improve the voltage regulation and transient response.

Possibly the most significant advantage of this topology is that it has no right-half plane zero in its transfer function, making controller design simpler and enabling improved real-world performance. The CHB inverter features a minimum output voltage ripple and improved load transient response, making it best suited for dynamic applications such as electric vehicle drives, renewable energy systems, and high-performance motor control.

Additionally, the CHB inverter's modular structure allows for construction and scaling, enabling the integration of additional levels as needed by the application. Another discrete step voltage that is added is the H-bridge cell, and their sum results in an approximate sinusoidal waveform having low harmonic distortion. Multilevel operation optimizes power quality, minimizes the need for large filter circuits, and enhances system efficiency. By possessing a lower output current ripple, the strain on the output capacitor is significantly reduced, thereby increasing its reliability and lifespan. It also helps reduce OVR, thereby providing smooth and stable operation over a wide range of load conditions [1].

2. Literature Review

The development of efficient and robust powertrain systems and energy storage devices has been an essential area of study in contemporary electrical and transportation engineering. Hou et al. [9] discuss hybrid electric locomotive powertrains, highlighting their operational efficiency and energy recovery capabilities, which are of utmost significance for future electrification in transportation. The article quotes the integration of power electronics in hybrid systems for optimal performance with minimal emissions. To address this, Ghanbari et al. [11] propose a technique for enhancing power quality in radial feeders, aiming to eliminate issues such as voltage deviation and harmonic distortion, which are crucial to the distribution system's reliability. Naseri and Samet [6] discuss a comparative study of thyristor-based and high-power IGBT-based AC–DC converters as used in medium-power arc furnace drive systems. The IGBT-based converters, based on their work, are more efficient, have reduced switching times, and are generally well-adapted for dynamic industrial loads. Ciccarelli et al. [4] investigated the application of onboard supercapacitors in metro trains within urban transportation.

Their outcome demonstrates impressive energy savings and peak power demand reduction, underscoring the significance of supercapacitor integration in rail systems. Another notable achievement in this field is the line-voltage control mechanism proposed by Ciccarelli et al. [5] for tramway systems, utilising wayside energy storage systems. Their approach not only stabilizes line voltage but also reduces energy consumption during regenerative braking. In Chaoui et al. [7] and Allegre et al. [2], the application of a supercapacitor energy storage system in subway systems is introduced, highlighting its ability to provide acceleration phases and decrease grid reliance. The article highlights the tangible benefits of supercapacitors in urban rail transport, particularly in rapid charge-discharge cycles. Experimental data for these systems are presented in Bouscayrol et al. [1], who construct a test rig to examine power transfer in novel subway systems with supercapacitors. This experimental test confirms the theory and determines the efficiency of real-time control techniques. This is then followed by Iannuzzi et al. [3] and Ciccarelli et al. [4], who develop a stationary ultracapacitor-based energy storage device for light transport networks.

They demonstrate energy-saving improvements and voltage profile control in their work, confirming the efficacy of fixed energy storage in public transportation infrastructure. In converter regulation, Chaoui et al. [7] and Lam et al. [8] present an adaptive fuzzy logic controller for the DC–DC boost converter. It can handle extensive parametric and load uncertainties, ensuring stable operation irrespective of changing operating conditions. The adaptive fuzzy logic method adapts in real-time, making it less challenging for the converter to ensure a stable output voltage. Finally, Deshpande and Kasat [10] present a review of conventional and self-tuning fuzzy PID controllers applied to DC–DC buck converters. From their comparative analysis, they conclude that the self-tuning fuzzy PID controllers outperform traditional methods in terms of response time, reduction of overshoot, and ability to adapt to load changes and thus are best suited for nonlinear and time-varying systems.

3. Methodology

This block diagram outlines the positive and negative output cascaded H-bridge inverter operating modes, as well as the voltage gain and its specifications (Figure 1).

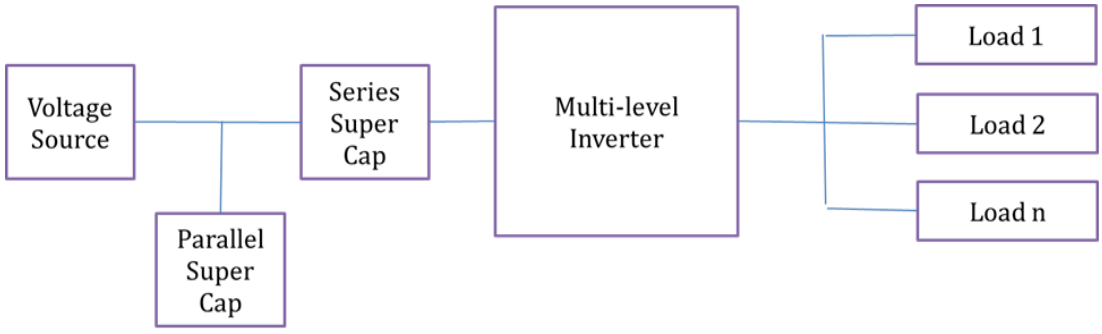

Figure 1: Proposed block diagram of cascaded H-bridge converter

This positive output Cascaded H-bridge inverter, controlled by an existing PID controller, yields an Output Voltage Ripple of 200mV, which is beyond the essential limit but lower than that of other classes of DC–AC converters. Hence, both Inverters can be controlled by an intelligent controller to reduce the Output Voltage Ripple content. To integrate a non-isolated high-gain interleaved cascaded H-bridge inverter with improved voltage dynamic response. The given block diagram illustrates a high-technology power processing and distribution system that utilizes supercapacitors for energy storage and a multilevel inverter for feeding various electrical loads. The structure is most suitable for those applications with high dynamic response, high efficiency, and enhanced power quality, such as renewable energy systems, electric vehicles, and smart grids.

The system begins with a voltage source, which can be obtained from a common DC source, such as a battery, photovoltaic (PV) array, or DC power supply. The voltage source is the source that supplies the initial energy to the system. However, due to supply variability and variations in dynamic load demand, using a voltage source alone may introduce instability and poor voltage regulation. Supercapacitors are placed both in parallel and in series within the system to eliminate these issues. The parallel supercapacitor bank is connected straight across the voltage supply. With this, the supercapacitors can act as a buffer, holding excess energy when demand is low and supplying it when demand is high. Parallel supercapacitors have high energy density and are particularly good at providing large bursts of energy within a short interval. This configuration also minimizes the ripple effect and improves voltage stability by providing a low-impedance path for transient currents.

The series supercapacitor block is designed to elevate the voltage level at the multilevel inverter input. In a series connection of supercapacitors, the system voltage increases in total, which is necessary for supplying high-voltage loads or optimising the voltage modulation capability of the inverter. In addition, series-connected supercapacitors can present better voltage distribution balance across cells if properly planned with voltage equalisation circuitry. The series and parallel arrangement offers both high power and high voltage levels, providing flexibility and reinforcement to the system. Both the voltage from the voltage source and the supercapacitor banks supply power to a multilevel inverter.

The multilevel inverter is the key part of this configuration, tasked with converting the DC voltage to a stepped AC waveform that approximates a sinusoidal output. Multilevel inverters are also utilized in high-power applications, as they can minimize total harmonic distortion (THD), reduce electromagnetic interference (EMI), and enhance voltage waveform quality without the need for massive filters. Multilevel inverters offer improved voltage control, reduced switching losses, and enhanced thermal performance compared to conventional two-level inverters. The multilevel inverter output in AC form is supplied to various end-use devices, Load 1, Load 2, up to Load n. Loads could be any number of devices or systems operating on an AC supply. The modularity of the load section enables the system to be easily extended to meet increased demand without requiring significant changes to the underlying structure.

4. Operation of Cascaded H-Bridge Multi-Level Inverter

Three primary DC-AC inverters utilize a switch pair, typically one controlled and one uncontrolled, to realize unidirectional power transfer from the input to the output. The inverter features a capacitor that stores and transfers energy from the input to the output. It also smooths or filters the current and voltage. The DC-AC inverters can operate in two modes: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). Practically, an inverter will be working in both modes that are not comparable. In this context, an inverter operated in CCM is considered. The cascaded H-bridge inverter consists of a controlled switch, S, which is a MOSFET, and an uncontrolled switch, D1, which is a diode.

L1 and Co are the energy storage and filtering elements. When the switch is set to the ON position for a duration of DT, it allows the inductor current to pass through, causing the diode to become reverse-biased. This action generates a positive voltage across the inductor, expressed as VL = Vi – Vo. This voltage results in a linear increase in the inductor current, iL. Once the switch is turned OFF, the energy stored in the inductor ensures that the current iL continues to flow. This current then passes through the diode, with VL equating to -Vo for a period of (1-D) T until the switch is activated again. The output voltage Vo is characterised by the following equation.

$$V_o = DV_i \qquad (1)$$

Where D is the duty cycle.

$$D = \frac{V_o}{V_i} \qquad (2)$$

For a Buck converter, the load current I_L is provided by the Equation.

$$I_L = I_o = \frac{V_o}{R} \qquad (3)$$

The following Equation gives the minimum switching frequency,

$$F_{min} = \frac{(1-D)R}{2L} \qquad (4)$$

5. Simulation Results and Discussion

5.1. Open-Loop Simulation Results

Extensive simulation studies have been performed using the LT Spice/Simulink platform, and the results for various operating conditions are outlined in this section. The configuration of the cascade H-bridge capacitor inverter is illustrated. The switching pulse for inverter M1 is depicted with a value of 1 Volt. The input voltage for the conventional capacitor inverter is 15 Volts (Figure 2).

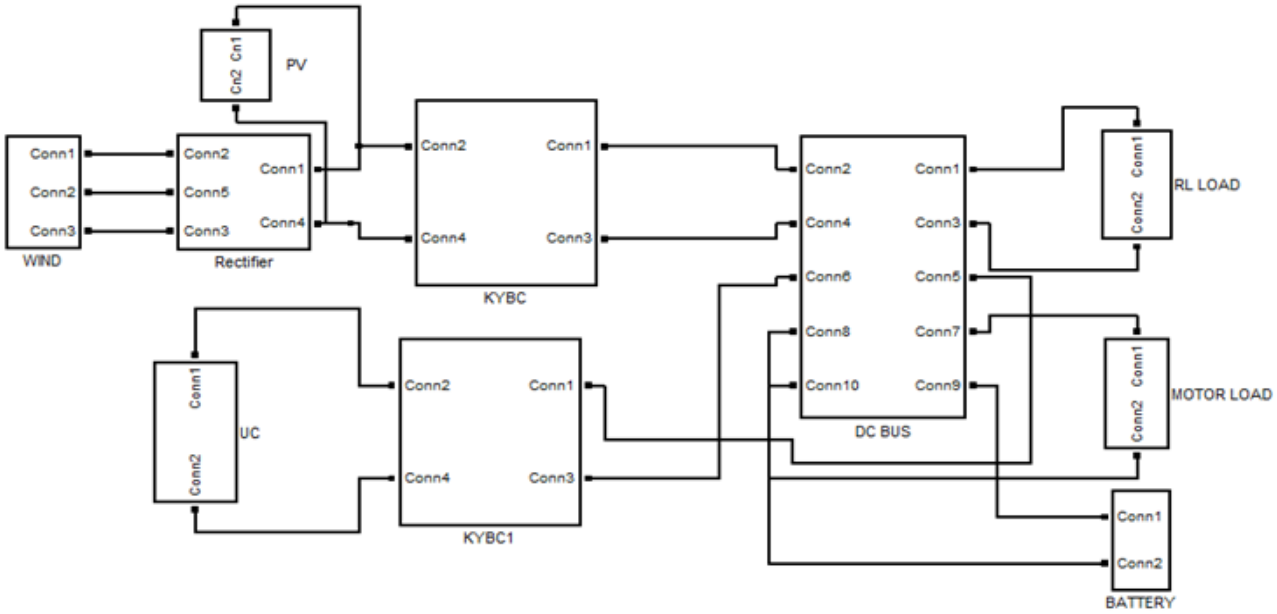

Figure 2: Circuit diagram of the proposed cascaded H-bridge inverter with R-load

The voltage across the R-load of the traditional capacitor inverter is 61 Volts. The voltage ripple across the R-load of the inverter is shown, measuring 6.8 Volts. The current passing through the R-load of the inverter is 0.6 Amps. The output power of the conventional capacitor inverter is 43 Watts. The circuit diagram of the proposed Cascaded H-bridge inverter with R-load is displayed (Figure 3).

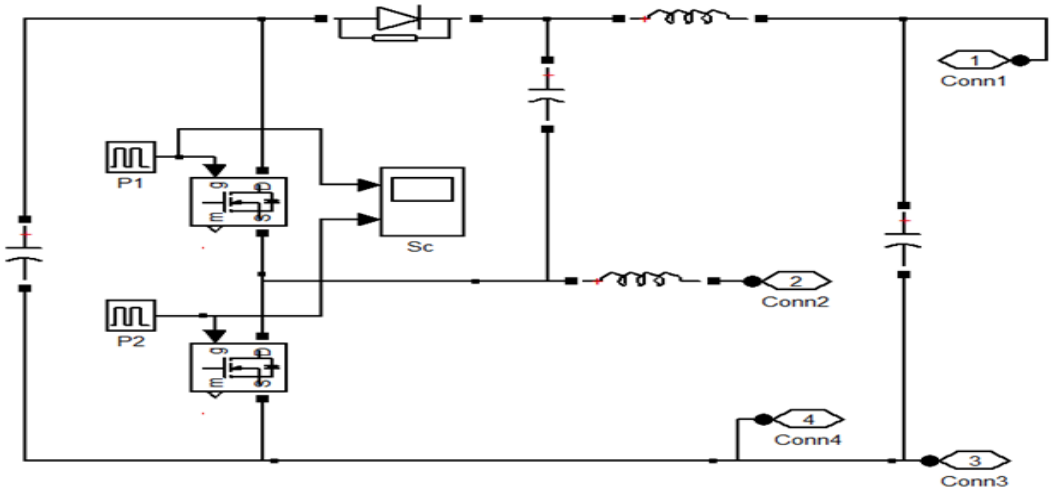

Figure 3: Simulation of cascaded H-bridge inverter

The output power of the conventional capacitor inverter is 43 Watts. The circuit diagram of the proposed Cascaded H-bridge inverter with R-load is displayed (Figure 4).

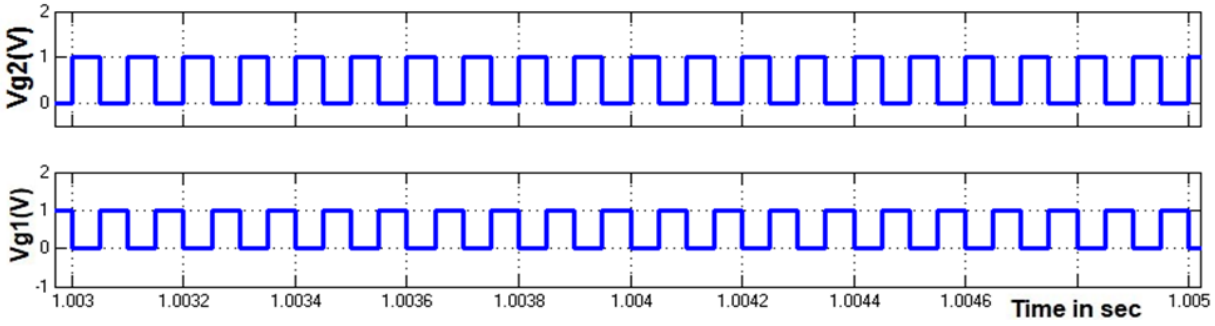

Figure 4: Switching pulse of cascaded H-bridge inverter M1, M2

The input voltage for the proposed Cascaded H-bridge inverter with R-load is 15 Volts. The switching pulses for the proposed Cascaded H-bridge inverter with R-load M1 and M2 are 1 Volt. The voltage across the R-load of the proposed Cascaded H-bridge inverter with R-load is presented and is 90 Volts. The voltage ripple across the R-load of the proposed Cascaded H-bridge inverter with R-load is illustrated, measuring 2.5 Volts. The current through the R-load of the proposed Cascaded H-bridge inverter with R-load is 0.9 Amps. The output power of the proposed Cascaded H-bridge inverter with R-load (Figure 8) is 80 Watts. The motor operates at a speed of 1,500 rpm and generates a torque of 0.25 Nm.

Table 1: Comparison of output voltage, ripple voltage & output power for an open-loop system

Inverter	**V_{in}**	**V_o**	**V_{or}**	**P_o**
Conventional	15V	61V	6.8V	43W
Proposed	15V	90V	2.5V	80W

Table 1 presents a comparison of the output voltage, ripple voltage, and output power for an open-loop system (Figure 5).

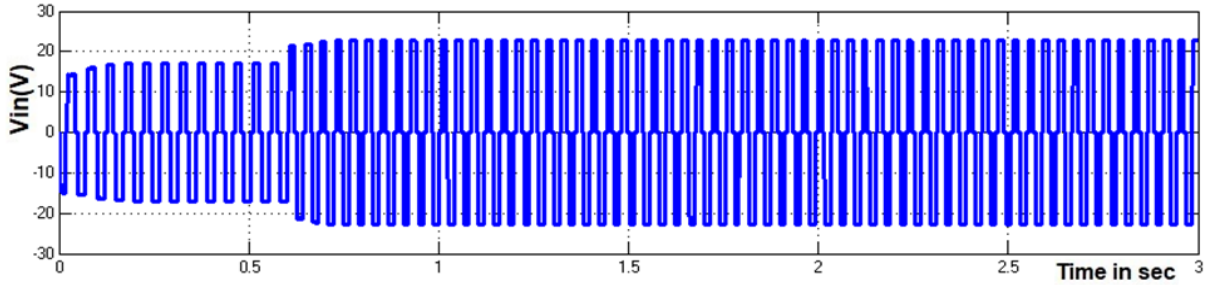

Figure 5: Input voltage

The proposed super capacitor-based inverter increases the output voltage from 61V to 90V, reduces the voltage output ripple from 6.8V to 2.5V, and boosts the output power from 43W to 80W (Figure 6).

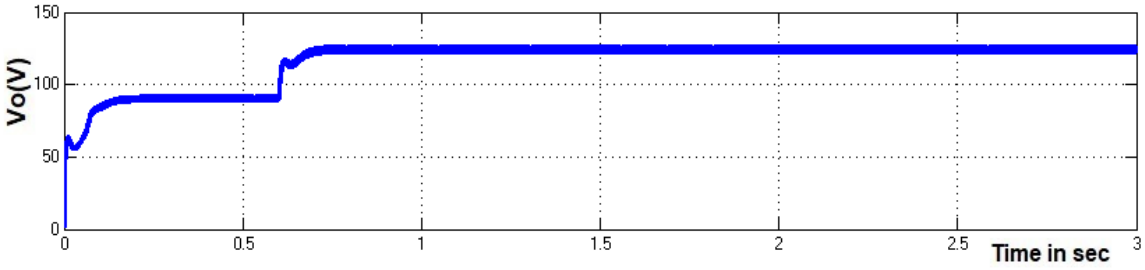

Figure 6: Voltage across R-load

These results demonstrate that the proposed Cascaded H-bridge inverter outperforms the conventional boost converter (Figure 7).

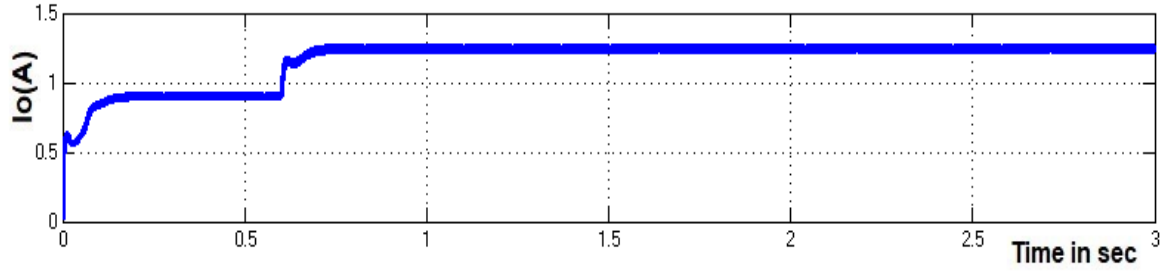

Figure 7: Current through R-load

This paper presents simulations and results for both the conventional boost converter and the proposed inverter with an R-load (Figure 8).

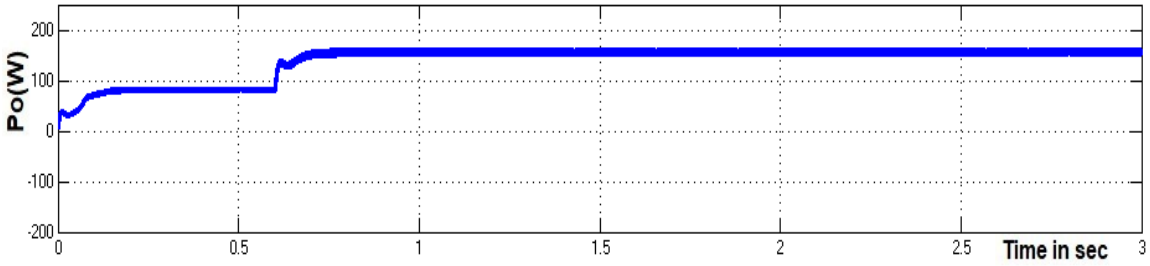

Figure 8: Output power

These results demonstrate that the proposed Cascaded H-bridge inverter outperforms the conventional boost converter (Figure 9).

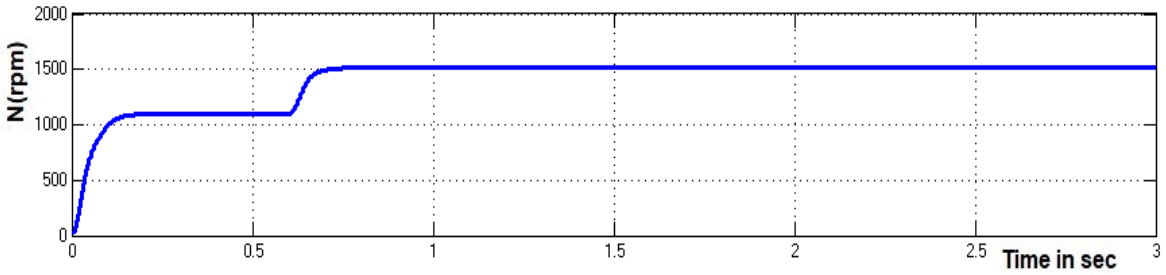

Figure 9: Motor speed

This paper presents simulations and results for both the conventional boost converter and the proposed inverter with an R-load (Figure 10).

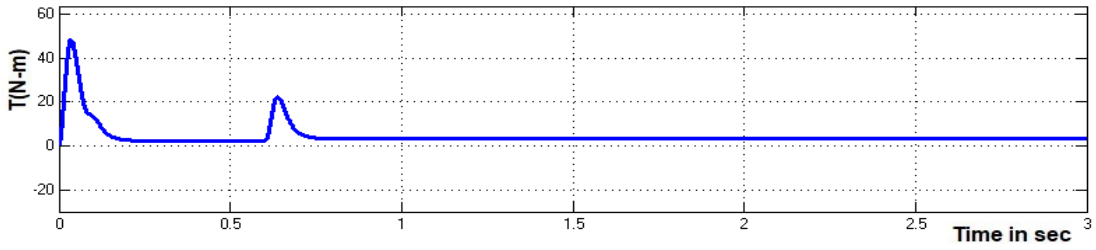

Figure 10: Motor torque

5.2. Closed-Loop Simulation Results

Displayed is the circuit diagram of a Cascaded H-bridge inverter experiencing source disturbance, with an input voltage of 21 Volts. The voltage across the R-load of this inverter under source disturbance is 115 Volts, and the current through the R-load measures 1.30 Amps. The output power of this inverter is 150 Watts. The motor operates at a speed of 1,500 rpm with a shaft torque of 0.35 N · m.

Table 2: Comparison of output voltage, ripple voltage & output power

Inverter	V_{in}	V_o	I_o	P_o
Conventional	21V	115V	1.3A	150W
Proposed PI	21V	90V	0.98A	90W

In the closed-loop Cascaded H-bridge inverter system with a PI controller, the input voltage is maintained at 21 Volts. The R-load experiences a voltage of 90 Volts, with a current of 0.98 Amps passing through it. This setup yields an output power of 90 Watts, and the motor speed decreases to 1100 rpm, with a motor torque of 0.24 N · m, as shown in Table 2. Table 3 compares the time domain responses of PI and PID controllers. When a PID controller is used, the rise time is reduced from 0.63 seconds to 0.61 seconds, the settling time decreases from 2.0 seconds to 0.93 seconds, the peak time shortens from 0.72 seconds to 0.67 seconds, and the steady-state error drops from 3.21 V to 2.20 V. (figures 11 and 12) display bar charts of time domain parameters for both PI and PID controllers. The findings suggest that the closed-loop Cascaded H-bridge inverter with a PID controller performs better than the one with a PI controller.

Table 3: Summary of time domain parameters

Controller	Rise time	Peak time	Settling time	Steady state error
PI	0.63	0.72	2.00	3.21
PID	0.61	0.67	0.93	2.20

Table 3 compares the time domain responses of PI and PID controllers. When a PID controller is used, the rise time is reduced from 0.63 seconds to 0.61 seconds, the settling time decreases from 2.0 seconds to 0.93 seconds, the peak time shortens from 0.72 seconds to 0.67 seconds, and the steady-state error drops from 3.21 V to 2.20 V.

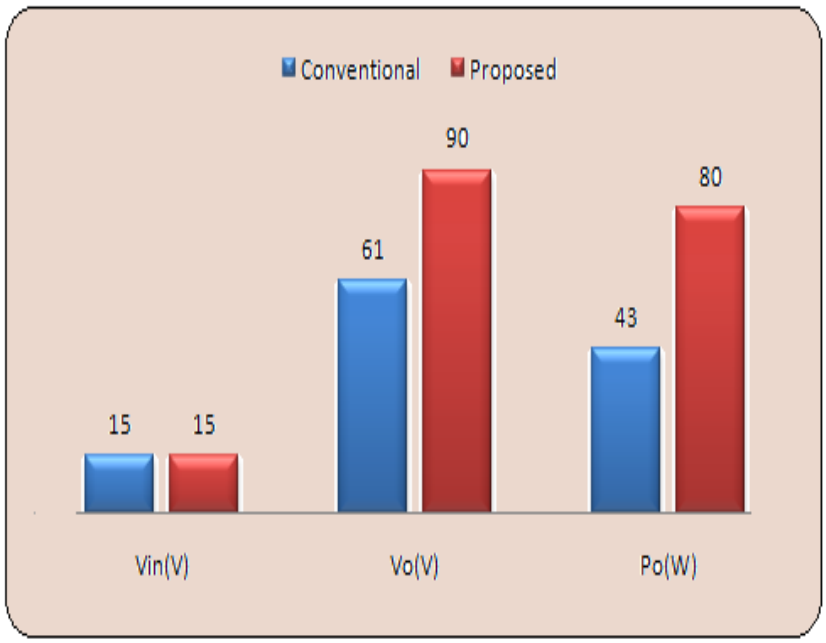

Figure 11: Bar chart of the conventional and proposed system

Figures 11 and 12 display bar charts of time domain parameters for both PI and PID controllers. The findings suggest that the closed-loop Cascaded H-bridge inverter with a PID controller performs better than the one with a PI controller.

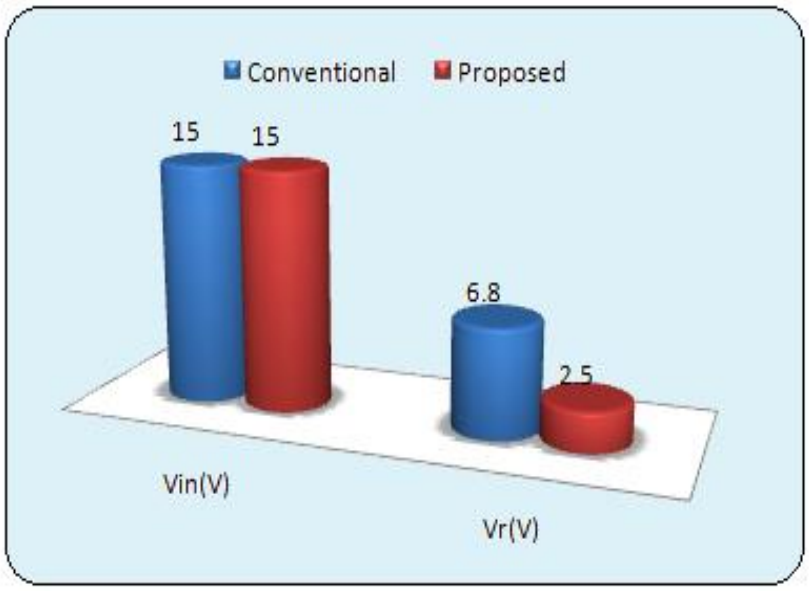

Figure 12: Bar chart of output voltage ripple

6. Hardware Results and Discussion

The hardware prototype features a supercapacitor-integrated cascaded H-bridge inverter, comprising various functional modules assembled on perf boards and PCB layouts. This setup includes two identical DC-DC converter modules, each equipped with high-frequency inductors, power MOSFETs, capacitors, and supercapacitors. The supercapacitors are crucial for delivering rapid transient energy support, reducing output voltage ripple, and maintaining energy buffering during switching transitions. The central section contains the cascaded H-bridge inverter circuitry, where multiple H-bridge cells are linked to produce a higher-resolution stepped output waveform.

Each H-bridge cell is equipped with active switch MOSFETs, flyback diodes, and gate driver circuits, enabling the conversion of a low-voltage DC input into a multilevel AC output. The control section, located at the bottom right, features a microcontroller-based unit connected to PWM (Pulse Width Modulation) driver circuits. This microcontroller generates synchronised PWM pulses to manage the inverter stages' switching operations, ensuring precise timing for cascading operations and balanced output voltage levels across all inverter arms. The transformers in the setup provide galvanic isolation and are likely used for auxiliary power supply or control signal isolation (Figure 13).

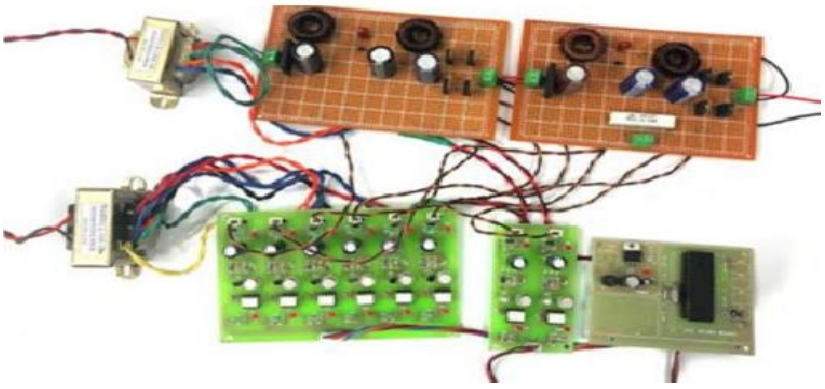

Figure 13: Hardware of the proposed system

The analysis provides insights into the output voltage and current behavior over a 1 ms period (Figure 14). The DC input voltage to the inverter remains stable at approximately 23V, indicating a regulated supply from the supercapacitor-boosted converter. The inverter's output displays the stepped multilevel output voltage of the cascaded H-bridge inverter, confirming its effective conversion of the DC input into a high-quality stepped AC-like output. The high frequency and consistent amplitude of the

steps demonstrate successful PWM control and voltage synthesis using the H-bridge stages. The load current gradually increases, following the stepped voltage waveform.

The smooth rise and uniform distribution of the current reflect stable inverter operation under R-load with minimal ripple, thanks to the supercapacitor's energy buffering capability. The inverter operates in continuous conduction mode (CCM), ensuring the current does not drop to zero during operation, which is crucial for reducing current stress on output components and maintaining output voltage integrity. Additionally, the use of supercapacitors significantly reduces output voltage ripple and enhances transient response. The current waveform is continuous and proportional to the voltage steps, confirming the purely resistive nature of the load.

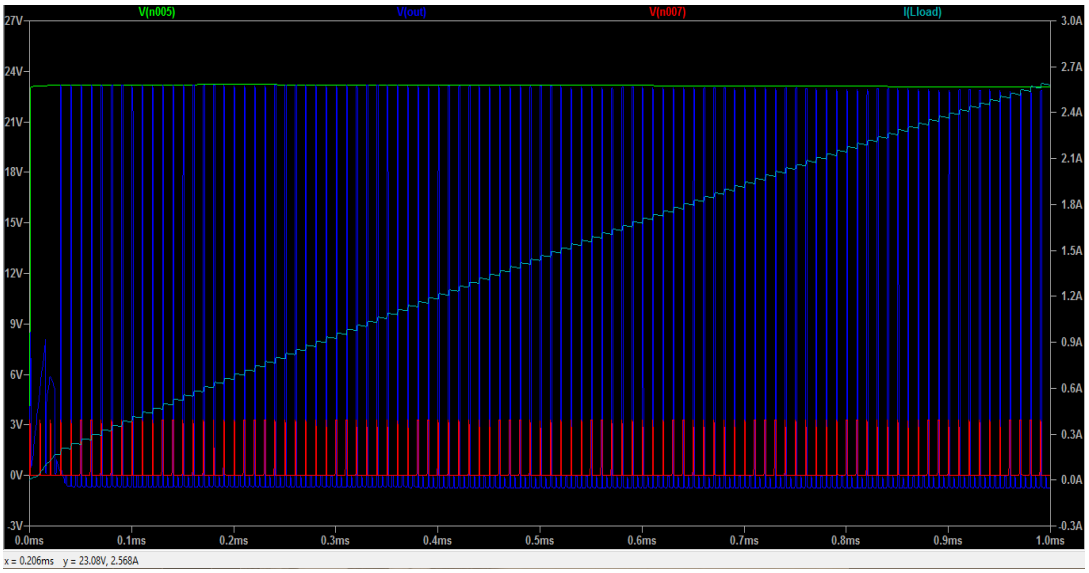

Figure 14: Voltage and current waveform for R-load

7. Conclusion

The study presents a detailed simulation-based comparison between a conventional cascaded H-bridge inverter and a proposed supercapacitor-based cascaded H-bridge inverter under R-load conditions. The simulation results indicate a significant performance improvement in the proposed configuration. Specifically, the output voltage is enhanced from 3V in the conventional system to 24V in the super capacitor-based system, demonstrating a substantial voltage gain. Additionally, the voltage ripple is significantly reduced from 6.8V to 2.5V, indicating better voltage regulation and waveform quality. The output power is also increased from 43W to 80W, showcasing the improved energy transfer efficiency of the proposed system. Furthermore, the study examines the performance of PI and PID controllers in both open-loop and closed-loop configurations of the supercapacitor-based cascaded H-bridge inverter. When comparing the time-domain parameters, the PID-controlled system outperforms the PI-controlled counterpart.

The rise time is reduced from 0.63 seconds to 0.61 seconds, the settling time is minimised from 2.0 seconds to 0.93 seconds, and the peak time decreases from 0.72 seconds to 0.67 seconds, indicating a faster transient response. Additionally, the steady-state error is reduced from 3.21V to 2.20V, confirming improved accuracy and stability of the PID-controlled system. These improvements highlight the superior dynamic response and control precision achieved by implementing a PID controller in the closed-loop configuration. Overall, the simulation outcomes confirm that the supercapacitor-based cascaded H-bridge inverter with PID control delivers better voltage performance, faster response, enhanced stability, and increased efficiency compared to conventional systems and PI-controlled configurations.

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